**REMARKS**

Claims 1-76 were pending. Claim 3 has been cancelled. Claims 24, 31, 35, 36, 54,55, 64, 68, 69 and 76 have been amended. Therefore, claims 1-2 and 4-76 remain pending subsequent entry of the present amendment.

Specification

Applicant has amended paragraph 0084 of the specification to incorporate subject matter appearing in original claim 3. No new matter has been added.

Claim Objections

Claim 24 has been amended to correct a typographical error.

Claim 31 has been amended in a manner which overcomes the objection regarding lack of antecedent basis.

Claim 54 has been amended in a manner which overcomes the objection regarding lack of antecedent basis.

The objection in paragraph 5 of the present Office Action is rendered moot due to the cancellation of claim 3.

35 U.S.C. § 112 Rejections

Claims 35, 55, 68 and 76 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Applicant's amendment to each of these claims is believed to overcome the rejection. The amendment to these claims is

supported throughout the description, including at paragraph 0088 which indicates the OS Domain Number field is capable of identifying root complexes or OS Domains.

Claims 3 and 36-39 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention. As claim 3 has been cancelled the rejection regarding claim 3 is rendered moot. The amendment to claim 36 is believed to overcome the rejection directed to claims 36-39.

35 U.S.C. § 102 and § 103 Rejections

Claims 1, 9-11, 13-19, 23, 25-26, 44, 48-49, 52-54, 56-57, 60, 69-73 and 75 stand rejected under 35 U.S.C. § 102(b)/(e) as being anticipated by U.S. Patent Publication No. 2002/0027906 (hereinafter "Athreya"). Claims 2-3, 12, 45-46, 51, 55, 61, 67-68, 74 and 76 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Athreya in view of U.S. Patent Publication No. 2004/0073716 (hereinafter "Boom"). Claims 4-8, 20-22, 24 and 47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Athreya in view of U.S. Patent No. 6,823,458 (hereinafter "Lee"). Claims 27, 28, 31, 33, 34, 36-43, 58, 59 and 62 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Athreya in view of U.S. Patent Publication No. 2004/0202013 (hereinafter "Dove"). Claims 29-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Athreya in view of Dove and in further view of Avery. Claims 32 and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Athreya in view of Dove and in further view of Boom. Claims 63-64 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Athreya in view of U.S. Patent No. 6,731,649 (hereinafter "Silverman"). Finally, claims 50, 65 and 66 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Athreya in view of U.S. Patent No. 6,834,326 (hereinafter "Wang").

Applicant respectfully traverses the above rejections and requests reconsideration in view of the following discussion.

Applicant notes each of the claim rejections depends upon at least the Athreya reference. However, Applicant submits the system disclosed by Athreya is completely different from that presently claimed and is inapposite. Generally speaking, Applicant's presently claimed invention is directed to systems and methods for sharing an endpoint within a load/store domain. As noted in the Description of the present application, modern computer architectures typically comprise distinct subsystems including a processing complex, an interface between the processing complex and I/O controllers or devices, and the I/O controllers or devices. Included in the following excerpt beginning on page 26 of the Description is one example that may serve to both clarify the nature of the presently claimed invention and distinguish the nature of the presently claimed invention from that of a prior art system.

> "Referring now to FIG. 4, a block diagram is shown of a multi-server environment 400 which incorporates shared I/O innovations of the present invention. More specifically three blade servers 404, 406, 408 are shown, each having one or more CPU's 410 coupled to their root complex 412. On the south side of the root complex 412 of each of the servers 404, 406, 408 are PCI Express links 430. The PCI Express links 430 are all coupled to a shared I/O switch 420 according to the present invention. On the south side of the shared I/O switch 420 are a number of PCI Express links 432 (defined below) coupled directly to shared I/O devices 440, 442, 444. . . .
>
> As will be further described below, none of the servers 404, 406, 408 have their own dedicated I/O controllers. Rather, the south side of their root complexes 412 are coupled directly to the shared I/O switch 420 which then allows each of the servers 404, 406, 408 to communicate with the shared I/O controllers 440, 442, 444 while still using the PCI Express load/store fabric. As more particularly shown, the shared I/O switch 420 includes one or more PCI Express links on its north side, a switch core for processing PCI Express data and instructions, and one or more PCI Express+ links on its south side for connecting to downstream PCI Express devices (such as network controllers, data storage controllers), and even another shared I/O switch 420 for cascading of PCI Express+ links. Further, each of the downstream devices 440, 442, 444 include a PCI Express+ interface 441, and Media Access Control (MAC). What should be appreciated by one skilled in the art, when comparing FIG. 4 to that shown in FIG. 2B, is that the three shared I/O devices 440, 442, 444 allow all three servers 404, 406, 408 to connect to the Ethernet, Fiber Channel, and Other

networks, whereas the solution of FIG. 2B requires nine controllers (three for each server) and three switches (one for each network type)." (emphasis added).

As can be seen from the above, a system is described wherein multiple root complexes are coupled to a shared switch which then allows sharing of I/O controllers – while still using the load/store fabric. In contrast, Athreya discloses a geographically distributed system and in no way concerns particulars of the operation within a given load/store domain.

With respect to the recited "root complex", in paragraph 8 of the present Office Action it is suggested that Athreya's disclosed networks (FIG. 2A, 3A) are equivalent to the recited root complexes. In view of the above, it should be apparent that the disclosed networks are not equivalent to the recited root complex. Further, as described on page 16 of the present application:

"Each of the servers 102, 104, 106 has a root complex 108. The root complex typically is the chip set which provides the interface between a processing complex (one or more CPU's which share a common memory and execute a common operating system), memory, and downstream I/O (e.g., IDE, SATA, Infiniband, Ethernet, Fiber Channel, USB, Firewire, PS/2). However, in the context of the present invention, the root complex may also include one or more processing complexes (processors+memory) as well as the other functions described above. Further, a root complex may include multiple processing complexes executing the same or different operating systems. For example, future processors may be designed which have multiple cores, each of which are independent of the other (i.e., each having its own memory structure and executing its own operating system). Within the context of PCI Express (which will be further discussed below), a root complex is a component in a PCI Express hierarchy that connects to the HOST bus segment on the upstream side with one or more PCI Express links on the downstream side. The present invention envisions all of these definitions for the term root complex."

Thus, "root complex" is described in a way which is believed clearly distinguishes from the networks disclosed by Athreya.

Additionally, claim 1 recites "a shared I/O switch coupled to said plurality of root complexes; and a shared I/O controller, coupled to said shared I/O switch." In the Office Action, it is suggested that switch 88 or router 90 of Athreya are equivalent to the disclosed "shared I/O controller". However, in view of the above discussion, it is believed clear that the disclosed switch or router are not equivalent to the recited I/O controller. As clearly described in the present application, one example of an I/O controller within the context of the present invention is a network interface controller (NIC). In view of the clarification regarding a "root complex" above, Athreya clearly does not disclose said shared I/O switch "places root complex identification within said packets for use by said shared I/O controller." In contrast, Athreya discloses a VLAN tagging unit (86) configured to create 802.1q VLAN frames. There is no disclosure of placing root complex identification within received packets.

Similar comments regarding the above distinctions are also applicable to claims 44, 57, and 72. Claim 27 recites features directed to operating system domains. In the Office Action, the rejection of claim 27 mirrors those of the other independent claims – with the exception of the citation of Dove for operating systems. However, it is believed clear from the above that the nature of the presently claimed invention is fundamentally different from that disclosed by Athreya, and merely indicating that the disclosed networks may comprise different operating systems does not produce an architecture as recited in claim 27.

As each of the independent claims has been rejected based upon Athreya, and Applicant has distinguished the claims from Athreya, all pending claims are patentably distinguished from the cited art for at least the reasons given above. While the dependent claims recite additional patentably distinct features, further discussion of such features is not believed necessary at this time.

Applicant believes the application to be in condition for allowance. However, should the examiner believe issues remain, the below signed representative would appreciate, and requests, a telephone interview to facilitate a resolution.

**CONCLUSION**

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

Respectfully submitted,

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